U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-12336 US	10/02/696
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Daniel C. Guterman et al.	
	Filing Date	Group
	October 31, 2001	2812

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	4,173,766	11/6/79	Hayes			
	AB	4,527,257	7/2/85	Cricchi			
	AC	4,622,656	11/11/86	Kamiya et al.			
	AD	4,870,470	9/26/89	Bass, Jr. et al.			
	AE	5,043,940	8/27/91	Harari			
	AF	5,070,032	12/3/91	Yuan et al.			
	AG	5,095,344	3/10/92	Harari			
	AH	5,168,334	12/1/92	Mitchell et al.			
	AI	5,172,338	12/15/92	Mehrotra et al.			
	AJ	5,313,421	5/17/94	Guterman et al.			
	AK	5,315,541	5/24/94	Harari et al.			

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL	EP 1 073 120 A2	1/31/01	Europe				
	AM	EP 1 091 418 A2	4/11/01	Europe				
	AN	EP 1 096 505 A1	5/2/01	Europe				
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AQ	Eitan et al., "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," IEEE Electron Device Letters, vol. 21, no. 11, November 2000, pp. 543-5.
	AR	Nozaki, "A 1-Mb EEPROM with a MONOS memory cell for a semi-conductor disk application," IEEE Journal of Solid State Circuits, vol. 26, no. 4, April 1991, p. 498.
	AS	Chan et al., "A true single-transistor oxide-nitride-oxide EEPROM device," IEEE Electron Device Letters, vol. EDL-8, no. 3, March 1987, pp. 93-95.

Examiner [signature] Date Considered 7/15/02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,343,063	8/30/94	Yuan et al.			
	AB	5,426,605	6/20/95	Van Berkel et al.			
	AC	5,436,481	7/25/95	Egawa et al.			
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	AF	5,712,180	1/27/98	Guterman et al.			
	AG	5,768,192	6/16/98	Eitan			
	AH	5,851,881	12/22/98	Lin et al.			
	AI	6,011,725	1/4/00	Eitan			
	AJ	6,030,871	2/29/00	Eitan			
	AK	6,091,633	7/18/00	Cernea et al.			

Foreign Patent Documents

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		Document	Date	Country	Class	Subclass	Yes	No
	AL							

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	AM	Eitan et al., "Hot-Electron Injection into the Oxide in n-channel MOS Devices," IEEE Transactions on Electron Devices, vol. Ed-28, no. 3, March 1981, pp. 328-340.
	AN	D. Frohman-Bentchkowsky, Applied Physics Letters, Vol. 18, 1971, page. 332.
	AO	D. Frohman-Bentchkowsky, "FAMOS - A new semiconductor charge storage device," Solid-State Electron., 1974, vol. 17. P. 517
	AP	Eitan et al., "Multilevel flash cells and their trade-offs," IEDM Tech. Dig., 1996, pp. 169-172.
	AQ	I. Fujiwara et al., "0.13 um MONOS single transistor memory cell with separated source lines," IDEM Tech. Dig., 1998, pp. 995-998

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	AA	6,103,573	8/15/00	Harari et al.			
	AB	6,104,072	8/15/00	Hirota			
	AC	6,137,718	10/24/00	Reisinger			
	AD	6,151,248	11/21/00	Harari et al.			
	AE	US 6,201,282 B1	3/13/01	Eitan			
	AF	US 6,215,148 B1	4/10/01	Eitan			
	AG	US 6,222,762 B1	4/24/01	Guterman et al.			
	AH	US 6,248,633 B1	6/19/01	Ogura, et al.			
	AI						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AJ							

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	AK	K. T. Chang et al., "A new SONOS memory using source-side injection for programming," IEEE Electron Device Lett., vol. 19, 1998, pp. 253-255.
	AL	P. J. Krick, "Three-state MNOS FET memory array," IBM Technical Disclosure Bulletin, vol. 18, no. 12, May 1976, pp. 1492-1493.
	AM	Takashi HORI et al., "A MOSFET with Si-implanted Gate-SiO_2 Insulator for Nonvolatile Memory Applications," IEEE, 0-7803-0817-4/92, pp. 17.7.1-17.7.4.
	AN	D. J. DiMaria et al., "Electrically-alterable read-only-memory using Si-rich SiO_2 injectors and a floating polycrystalline silicon storage layer," J. Appl. Phys., 52(7), July 1981, pp. 4825-4842.
	AO	"Basic Programming Mechanisms," Nonvolatile Semiconductor Memory Technology - A Comprhensive Guide to Understanding and Using NVSM Devices, IEEE Press series on microelectronic systems, 1998, pp. 9-25.
	AP	Kamiya, M., et al., "EPROM Cell With High Gate Injection Efficiency," International Electronic Devices Meeting of IEEE, San Francisco, California, (Dec. 13-15, 1982) pps. 741-744

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